Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-26. Canceled

Claim 27. (Currently amended) An electronic system comprising:

an integrated circuit comprising:

an output buffer comprising a pull-up transistor coupled between a pad and a first supply voltage;

a first transistor coupled between a bulk of the pull-up transistor and a source of the pull-up transistor, and having a gate coupled to receive a control signal; and

a second transistor coupled between a drain of the pull-up transistor and the bulk of the pull-up transistor, and having a gate coupled to receive a complement of the control signal;

a hot-socket circuit coupled to the pad and the first supply voltage, wherein the hot-socket circuit provides an output having a first state if a voltage on the pad is higher than the first supply voltage and a second state if the voltage on the pad is lower than the first supply voltage; and

a logic circuit coupled to receive the output of the hot-socket circuit and an enable signal and to provide the control signal,

wherein when the control signal is in a first state, the bulk of the pull-up transistor is coupled to the pad, and when the control signal is in a second state, the bulk of the pull-up transistor is coupled to the first supply voltage, and a drain-to-bulk diode of the pull-up transistor clamps a voltage received at the pad, and when the enable signal is in ~~a disable~~ an enable state, the bulk of the pull-up device is coupled to the first supply voltage, and when the enable signal is in a disable state, the bulk of the pull-up device is coupled to the higher voltage of the pad or the first supply voltage.

Claim 28. (Previously presented) The electronic system of claim 27 further comprising:

a resistor coupled to the pad and further coupled to receive an input signal.

Claim 29. (Previously presented) The electronic system of claim 28 wherein the integrated circuit further comprises:

an input buffer coupled between the first supply voltage and a second supply voltage and having an input directly connected to the pad.

Claim 30. (Previously presented) The electronic system of claim 28 wherein the logic circuit is an AND gate.

Claim 31. (Previously presented) The electronic system of claim 28 wherein the integrated circuit further comprises:

a plurality of programmable logic elements configurable to implement user-defined logic functions.

Claims 32-35 (Canceled)

Claim 36. (New) An integrated circuit comprising:

a pull-up MOS transistor coupled between a first supply voltage and a pad;

a pull-down MOS transistor coupled between the pad and a second supply voltage that is lower than the first supply voltage;

a first MOS transistor switch having a source/drain terminal coupled to the first supply voltage;

an active diode having a first terminal coupled to the drain/source terminal of the first MOS transistor switch, and a second terminal coupled to the pad; and

a biasing circuit adapted to apply to bulk regions of the pull-up MOS transistor and the first MOS transistor switch the higher of a voltage applied to the pad and the first supply voltage.

Claim 37. (New) The integrated circuit of claim 36 further comprising:

an input buffer coupled directly to the pad.

Claim 38. (New) The electronic circuit of claim 36 further comprising:

a first predriver circuit coupled to a gate terminal of the pull-up MOS transistor; and

a second predriver circuit coupled to a gate terminal of the pull-down MOS transistor.

39. (New) An integrated circuit comprising:

a pull-up MOS transistor coupled between a pad and a first supply voltage;

a pull-down MOS transistor coupled between the pad and a second supply voltage that is lower than the first supply voltage;

a first MOS transistor switch having a source/drain terminal coupled to the first supply voltage;

a second MOS transistor switch coupled between the first MOS transistor switch and the pad, the second MOS transistor switch having a bulk terminal coupled to the bulk terminal of the first MOS transistor switch and a common source/drain terminal of the first and second MOS transistor switches;

a comparator circuit coupled to the pad and the first supply voltage, wherein the comparator circuit provides an output having a first state if a voltage on the pad is higher than the first supply voltage and a second state if the voltage on the pad is lower than the first supply voltage; and

a first logic block configured to perform logical AND operation and responsive to output signal of the comparator circuit and an enable signal; and

a second logic block configured to perform logical inversion operation and responsive to the first logic block, the second logic block disposed between gate terminals of the first and the second MOS transistor switches.

Claim 40. (New) The electronic circuit of claim 39 further comprising:

a first predriver circuit coupled to a gate terminal of the pull-up MOS transistor; and

a second predriver circuit coupled to a gate terminal of the pull-down MOS transistor.

Claim 41. (New) An electronic system comprising:

an integrated circuit comprising:

a pull-up MOS transistor coupled between a first supply voltage and a pad;

a pull-down MOS transistor coupled between the pad and a second supply voltage that is lower than the first supply voltage;

a clamp MOS transistor having a source/drain terminal coupled to the first supply voltage and a gate coupled to a control signal;

a diode having a first terminal coupled to the drain/source terminal of the clamp MOS transistor, and a second terminal coupled to the pad;

a biasing circuit coupled to provide the higher voltage between a voltage on the pad and the first supply voltage to a well of the pull-up MOS transistor and the clamp MOS transistor; and

a resistor external to the integrated circuit.